RESEARCH DEPARTMENT

Pulse-code modulation for high-quality sound signal distribution: coding and decoding

TECHNOLOGICAL REPORT No. EL-18

UDC 534.86: 621.376.56 1968/29

THE BRITISH BROADCASTING CORPORATION
ENGINEERING DIVISION

RESEARCH DEPARTMENT

PULSE-CODE MODULATION FOR HIGH-QUALITY SOUND SIGNAL DISTRIBUTION: CODING AND DECODING

Technological Report No. EL-18
UDC 534.86: 1968/29
621.376.56

It uses SI units in accordance with B.S. document PD 5686.

J.R. Chew, B.Sc.(Eng.), C.Eng., M.I.E.E.

Head of Research and Development

Technological Report No. EL-18

PULSE-CODE MODULATION FOR HIGH-QUALITY SOUND SIGNAL DISTRIBUTION: CODING AND DECODING

July 1968

Technological Report No. EL-18
UDC 534.86: 1968/29
621.376.56

PULSE-CODE MODULATION FOR HIGH-QUALITY SOUND SIGNAL DISTRIBUTION: CODING AND DECODING

SUMMARY

The various methods for converting analogue signals into the form of pulse-code modulation and back again are reviewed.

Reasons are given for preferring a particular method of conversion called 'counter conversion' which is particularly suitable for sound signals.

Equipment for coding and decoding high-quality sound signals using the 'counter' type of converter has been constructed and its design and performance is described.

1. INTRODUCTION

In the first report of this series[1] the present and probable future state of the BBC sound signal distribution network, which is rented from the G.P.O., was considered. The conclusion was drawn that in order to take advantage of the economies afforded by modern wideband communication techniques the traditional baseband 'music line' system will not be extended, and will indeed contract as existing lines reach the end of their useful life. In the immediate future the BBC must make increasing use of other types of G.P.O. circuit, many of which are not entirely satisfactory. However the G.P.O. plan to make increasing use of pulse-code modulation, and this form of transmission has been shown to be very promising for the transmission of broadcast-quality sound signals.[1] In order to make use of this transmission technique suitable coding and decoding equipment will be needed.

The purpose of this report is to assess the various methods by which sound signals may be converted to and from binary p.c.m. and to describe recent work carried out by Research Department in this field.

Processing of high-quality audio signals for transmission by digital methods depends upon the availability of suitable analogue-to-digital converters, (a.d.c.) and digital-to-analogue converters (d.a.c.). Converters for this purpose require a particular combination of speed and amplitude resolution which is not demanded in other applications. The requirements for digital transmission of high-quality audio signals have already been stated in Reference 1 to be (a) that the signal should be sampled at a rate of approximately 30 kHz, that is, a 30 kHz word rate in transmission, and (b) that the ratio of peak signal to peak weighted quantizing noise* should be at least 60 dB, which implies the use of an 11-bit word and an incremental coding accuracy of 0·05%.

The above criteria are based upon the use of p.c.m. with uniform quantizing steps. Non-linear coding techniques, involving graduated quantizing steps and intended to reduce the required bit rate, are not considered in this report.

2. FUNDAMENTAL AND INSTRUMENTAL CAUSES OF CODING AND DECODING ERRORS

The process of quantizing a continuum of input signal values into a finite set of codes implies coding errors. The total range of the possible errors is equal to the difference between two successive quantizing levels. The effect on the reconstituted signal is to add to it a flat frequency-spectrum noise called 'quantizing noise' which differs from Gaussian 'white noise' only in having a rectangular probability-density.

In theory, adding an extra binary digit to the code, thereby doubling the number of quantizing

* This method of specifying signal-to-noise ratio is currently used in connection with the BBC sound distribution network (see appendix to Reference 1).

levels and halving the separation between successive levels, should reduce the quantizing noise by 6 dB. In practice the expected reduction in noise level with each additional bit in the code is achieved only up to the point at which inaccuracies in the converters become appreciable. The most obvious cause of inaccurate coding and decoding is errors in the analogue circuits – both signal and reference circuits can produce errors of this kind.

A less obvious but equally important cause of inaccuracy in decoding equipment is timing error. Jitter on the timing of the samples taken by the coder causes an error proportional to the rate of change of the input signal. Timing jitter in the decoder which modulates the width and/or position of the amplitude-modulated pulses at the output of the decoder will also produce noise components in the reconstituted signal. For example, in a p.c.m. system sampling at 30 kHz, coding an 11-bit word, a pulse width error of 16·3 ns in the d.a.c. output would produce a noise voltage equal to the contribution to the signal of the least significant bit.

Because of the possibility of errors within the coding and decoding equipment it is necessary to measure the level of noise in the recovered analogue signal and by comparison of the theoretical and measured values establish the merit of the equipment.

Quantizing noise exists only in the presence of a signal, and therefore special techniques are needed in order to measure it. One method relies upon the use of a signal whose spectrum occupies a restricted portion of the base bandwidth. The quantizing noise produced within that portion of the base bandwidth which is not occupied by the signal is then measured. In another method thermal noise injected into a parallel reference circuit having the same gain as the p.c.m. chain is adjusted by ear, in the presence of programme, to be equal in loudness to the quantizing noise. The level of the injected noise in the reference chain is then measured in the absence of signal. It has been found that the adjustment of injected noise to equality with the p.c.m. noise can be easily repeated to within ± 1 dB.

The remaining sections of this report are concerned with the basic principles of coding and decoding and with the development of equipment suitable for use with high-quality sound signals.

3. CODING METHODS USED IN ANALOGUE-TO-DIGITAL CONVERTERS

A large number of analogue-to-digital conversion methods is known but all derive from three basic methods according to the way in which the amplitude of the signal sample is measured. Converters of the first kind compare the voltage of the signal sample with a number of precise voltage levels presented successively in descending order of magnitude; each level corresponds to the magnitude signified by one digit position in the code. As soon as a level is reached which is less than the voltage of the sample, subtraction takes place and a '1' is generated for that digit position; the difference signal is then dealt with in the same way and the process is repeated until all the digit positions have been explored. This method is known as successive-approximation conversion.

In converters of the second kind the amplitude of the sample is measured by counting out the number of units contained in it until less than one remains. This may be done by comparing the signal sample with a uniformly rising ramp; during the ramp period a counter runs at constant speed and accumulates a number proportional to time. When the ramp voltage equals the sample voltage the counter is stopped and the converter output read from the counter.

In the third kind of converter, known as a 'parallel converter' the sample amplitude is measured by comparing its voltage simultaneously with the complete set of possible quantized values. As already indicated, the coding of high-quality sound signals requires high incremental accuracy; this requirement eliminates parallel-converters because of the complexity and expense of a circuit containing the extremely large number of comparators which would be required.

4. DECODING METHODS USED IN DIGITAL-TO-ANALOGUE CONVERTERS

Three essentially different methods of decoding are known. The first of these was described by Oliver, Pierce and Shannon in 1948[2] and is applicable to binary code only. The binary number to be decoded is presented in reverse order, i.e. with the least significant bit first and the most significant bit last. The reception of each bit in turn by the converter causes a fixed charge to be injected into the capacitor of a parallel capacitor-resistor circuit, the time constant of which is so adjusted that the voltage across the capacitor decays to half its value in the time interval between successive bits. The capacitor voltage immediately after reception of the last (most significant) bit is then directly proportional to the binary number.

In the second method a time interval is counted out proportional to the digital number to be decoded.

During this time interval a linear process, for example the charging of a capacitor by a constant current, is allowed to proceed. At the end of the time interval the accumulated quantity, e.g. the voltage on the capacitor, is proportional to the time interval and thus to the digital number being decoded. This decoding method bears a close relationship to counter coding.

For the third method of decoding, the digital number to be converted is first assembled in a holding register. When the number is complete a 'command' pulse applied to gating circuits causes each digit representing '1' to turn on a current proportional to the value signified by that digit. The sum of the currents is then proportional to the digital number. This method of decoding corresponds roughly to the parallel or 'simultaneous coding' process.

5. CHOICE OF CODING AND DECODING METHODS

In certain respects the requirements for audio-signal transmission are far less stringent than those for, for example, data transmission. For audio signals, slowly-varying errors of signal amplitude up to about ± 5% are tolerable, and the fact that the audio-frequency band does not extend to zero frequency implies that direct current injected into the signal chain as a by-product of coding and decoding is unimportant.

To produce the most economic design of a p.c.m. system for audio signals the relaxations above should be fully exploited and the coding and decoding methods adopted should of their very nature provide the theoretical quantizing noise level with the minimum of pre-set adjustments. In the counter methods, discussed in Sections 3 and 4, the output of the converter is monotonically related to the input. No discontinuities can occur in the conversion law because no sets of current or voltage references requiring accurate adjustment are used, an advantage shared by no other coding method.

For these reasons the counter method of coding and decoding was adopted for the sound-signal converters described below.

6. THE DESIGN OF A COUNTER-TYPE ANALOGUE-TO-DIGITAL CONVERTER

Fig. 1 shows a schematic of a counter-type a.d.c.; the clock rates shown are appropriate to 11 bits and a sampling rate of approximately 30 kHz.

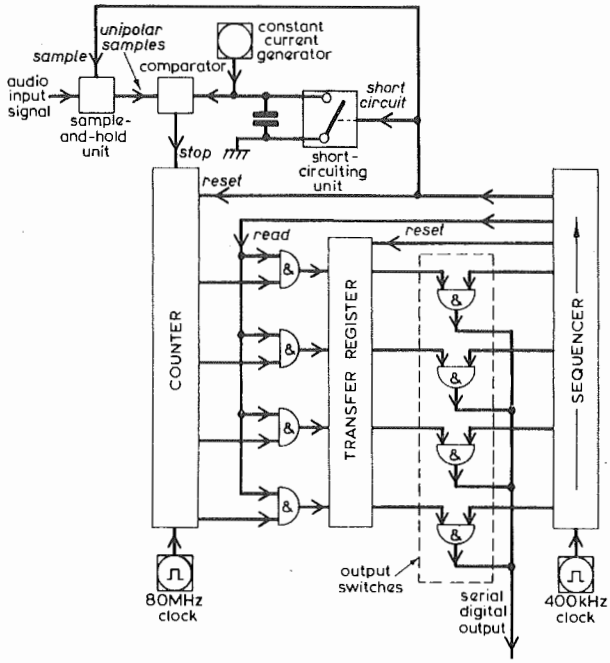

Fig. 1 - Counter-type analogue-to-digital converter block diagram (4 bits only shown for simplicity)

The input signal is sampled and held and applied to one input of a voltage comparator. The other input to the comparator is provided by a voltage across a capacitor which is being charged from a constant current source. In the initial state, up to the moment the sample is applied, the capacitor is short-circuited and the counter is held in the reset condition. The short-circuit across the capacitor and the reset signal on the counter are then simultaneously removed; the capacitor then begins to charge and the counter begins to count the pulses supplied by the 80 MHz clock. When the voltage across the capacitor equals the voltage of the applied sample, a pulse from the comparator stops the counter and the required digital representation of the input voltage sample is then available at the counter outputs.

The time interval between successive samples at 30 kHz sampling rate is 33·3 μs. The counting process described above occupies a period of time proportional to the number produced but in all cases must be complete sufficiently quickly to allow the digital output to be read and the counter and capacitor voltage to be reset in time for the next conversion. The need to provide an 11-bit digital output implies a maximum count of 2048, which, with a counting rate of 80 MHz, will be complete in 25·6 μs.

The remainder of the a.d.c. is concerned only with storing the digits, reading them out in the proper sequence for transmission and resetting the circuits ready for the next conversion. The

sequence of control operations in the coder is dictated by a sequencer driven by a 400 kHz clock, and this clock determines the 'bit-rate' or rate at which the pulses comprising the digital signal leave the a.d.c. The 400 kHz bit-rate clock requires to be synchronized with the 80 MHz counter-driving clock, since the 400 kHz clock controls the moment when conversion begins. The start of counting must always occur synchronously with respect to the 80 MHz clock, or a random error would occur, the peak-to-peak amplitude of which would equal one quantum level. In practice, therefore, the 400 kHz pulses are derived from the 80 MHz pulses by frequency division.

Propagation delays in the comparator result only in the addition of a constant number to the generated code and hence in the addition to the reconstituted signal of a d.c. component which is easily removed at the analogue output. Propagation delays in the short-circuiting device and the release circuitry of the counter have a similar effect, as does imperfect short-circuiting of the capacitor, the result of which would be to leave a small initial charge.

Slow variation with time of the nominally constant current charging the capacitor will change the magnitude of the signal slightly. Both these errors are acceptable in moderate amounts. The critical requirement of monotonicity in the conversion is intrinsic in the coding method.

One instrumental requirement which became apparent during the experimental work was the necessity of preventing overrun in the counter of the coder at maximum signal excursion. If allowed to overrun the counter would suddenly revert to zero and then start to count up again. The result is a particularly violent overload condition in which overloading peaks of signal are transferred to the opposite extreme of the signal range with aurally disastrous consequences. Logic circuits may be connected to the counter to prevent any digits of more than a particular significance from being changed after they have all become '1'. This artifice ensures that if the counter subsequently overruns only digits of low significance can be removed. By proper choice of the disconnection point the undesirable overload characteristic can be suppressed to any required degree.

7. DESIGN OF A COUNTER-TYPE DIGITAL-TO ANALOGUE CONVERTER

The considerations leading to the adoption of a counter-type coder lead with equal force to the adoption of a counter-type decoder. The two instruments, although they have much in common, differ in a number of respects. The design of a counter-type decoder is described below.

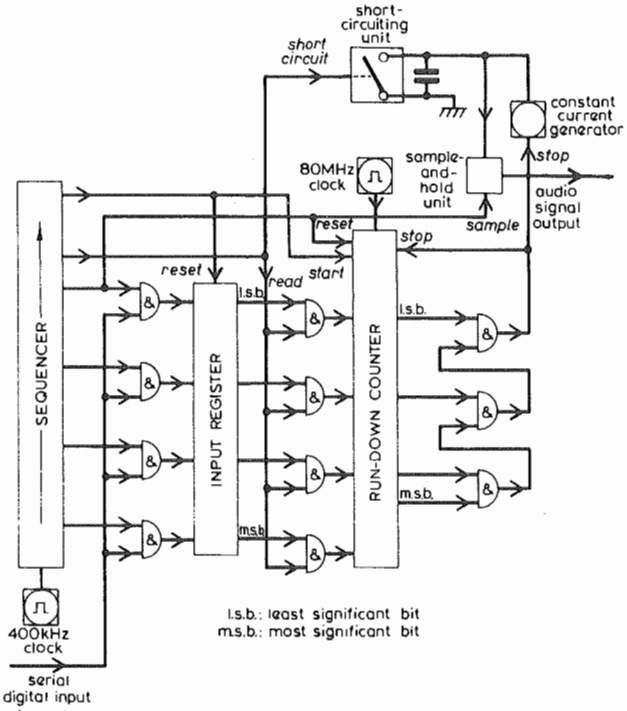

Fig. 2 - Counter-type digital-to-analogue converter block diagram (4 bits only shown for simplicity)

Fig. 2 shows a schematic of a counter-type d.a.c. corresponding to the coder discussed in Section 7. Here the number to be decoded is set into a high-speed counter using presetting connections on the counting stages. After setting the counter, counting is started and a capacitor simultaneously begins to charge from a constant current source. The counter then counts down to zero under the control of an 80 MHz clock; the final transition to an all-zeros state, involving only the bistable stage for the least significant bit, stops the charging of the capacitor. The voltage on the latter is then proportional to the number being decoded and when sampled and filtered provides the analogue output.

The action of the counter d.a.c. as described in the simple explanation given above, is correct in principle but requires in practice a small modification to keep within the operating speed of currently available integrated circuits. The difficulty arises because the stop signal, as generated by the last bistable element in the counter, exists for only a very short time. Fortunately, by deriving the stop signal from the second or third bistable, its duration can be doubled or redoubled; thus, in a counter running at 80 MHz the duration of the stop signal can be increased from 12½ to 25 or 50 ns, a length of time sufficient to operate the counter-

stopping circuits reliably. It should be noted that a penalty is incurred by the use of this artifice in that the counter will be stopped before it reaches zero. If the stop signal is derived from the 9th digit and 11 are provided, the counter will be stopped at the time when the number $2^{(11-9)}-1$ remains. Thus in the case of an eleven-bit decoder the number of usable levels will be reduced from 2048 to 2045 which is negligible in practice.

The remarks made about tolerance of the audio signal to timing and capacitor starting voltage errors when discussing the counter-type a.d.c. are also applicable to the counter-type d.a.c.

8. SYNCHRONIZATION OF THE CODING AND DECODING PROCESSES

During experimental use of the coding and decoding equipment described in this report, the d.a.c. was synchronized to the a.d.c. by a separate connection carrying synchronizing pulses from one to the other. Extraction of a synchronizing signal from the groups of transmitted digits was not attempted.

Nevertheless the use of separately transmitted pulses to synchronize the d.a.c. is not entirely straightforward, as the decoding process is controlled by pulses derived from an 80 MHz clock. In the steady-state condition the phase of the synchronizing pulse is compared with a d.a.c. sequencer pulse and the error signal applied to correct the frequency of the d.a.c. clock.

The stability of the d.a.c. clock is such that the time required to achieve initial synchronism, or to re-establish synchronism after a disturbance, would be unacceptably long if it were achieved by clock-frequency control alone. To overcome this defect a circuit is provided which, should synchronism be lost, halts the d.a.c. at that point in its operating cycle which should coincide with the arrival of a synchronizing pulse and re-starts it when the next synchronizing pulse arrives.

9. PERFORMANCE OF COUNTER A.D.C. AND D.A.C.

The ultimate limitation on the performance of coders and decoders must lie with the analogue circuits involved; in counter instruments, in particular, it depends on the consistency and precision of the sample-and-hold, ramp, and comparator circuits as well as on the limit of discrimination of the comparator.

The signal-to-noise ratio of the present a.d.c. or d.a.c. connected in tandem, measured by the noise substitution method of Section 2, was found to equal the theoretical value within the limits of experimental error (± 1 dB), indicating that the performance of the analogue circuits involved was adequate for 11-bit coding.

As confirmation of the adequacy of the analogue circuit noise level a measurement was made of the timing stability of the stop pulse from the comparator of the a.d.c. when coding repeatedly a steady applied voltage. The timing jitter visible on the stop pulse was approximately 3 ns. Since the counting rate for 11 bits is one count in 12·5 ns this indicates that the analogue circuits at present in use would be suitable for 12-bit coding, i.e. coding with a counting rate of 6·25 ns per count.

10. CONCLUSION

This report has outlined the three basic methods of coding and decoding which could be applied to p.c.m. transmission of audio signals. Reasons pointing to the selection of counter-type coding and decoding have been given and some of the less immediately apparent difficulties of all coding methods have been discussed.

Counter-type instruments both for coding and decoding audio signals of broadcast quality have been developed and their performance found to be satisfactory. The counting frequencies involved are high by present-day standards, and are near to the fastest that can be achieved by modern integrated circuits. However, at the present rate of progress of integrated circuit performance, such high counting speeds are likely to become commonplace within a short time. With this prospect in view it is felt that counting methods will provide the cheapest method of conversion available in the near future and, further, will require the minimum of maintenance and adjustment.

11. REFERENCES

1. Pulse-code modulation for high-quality sound-signal distribution: appraisal of system requirements. BBC Research Department Report No. EL-10, Serial No. 1967/50.

2. OLIVER, B.M., PIERCE, J.R. *and* SHANNON, C.E. 1948. The philosophy of P.C.M. *Proc. Inst. Radio Engrs.*, 1948, **36**, 11, pp. 1324-1331.

JMP

Printed by BBC Research Department, Kingswood Warren, Tadworth, Surrey